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(54) **STRAINED STRUCTURE OF SEMICONDUCTOR DEVICE AND METHOD OF MAKING THE STRAINED STRUCTURE**

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(51) **Int. Cl.**

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H01L 29/66	(2006.01)
H01L 29/10	(2006.01)
H01L 29/165	(2006.01)
H01L 21/8238	(2006.01)
H01L 21/02	(2006.01)

(52) **U.S. Cl.**

CPC .. ***H01L 29/66636*** (2013.01); ***H01L 21/823807*** (2013.01); ***H01L 21/823814*** (2013.01); ***H01L 21/823821*** (2013.01); ***H01L 21/823878*** (2013.01); ***H01L 27/0924*** (2013.01); ***H01L 29/1054*** (2013.01); ***H01L 29/165*** (2013.01); ***H01L 29/66651*** (2013.01); ***H01L 29/7848*** (2013.01); *H01L 21/0262* (2013.01); *H01L 21/02532* (2013.01)

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CPC H01L 27/092; H01L 29/78; H01L 21/02; H01L 21/20; H01L 29/242; H01L 29/772; H01L 31/119; H01L 31/0304; H01L 29/12; H01L 29/20

USPC 257/369, 288, 192, 256, 408, 327, 407, 257/344, 412

See application file for complete search history.

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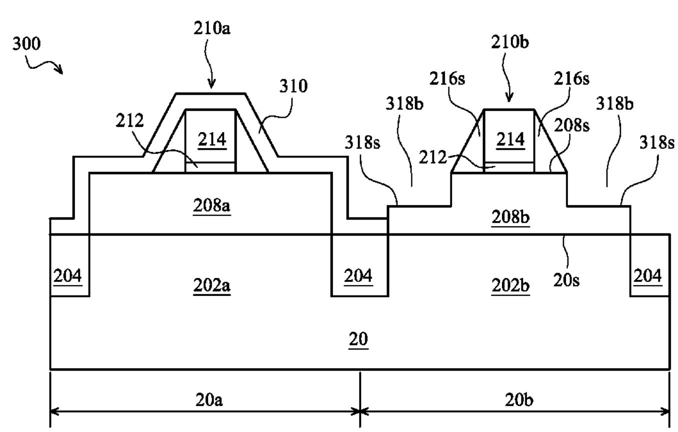
(57) **ABSTRACT**

An exemplary structure for a field effect transistor (FET) comprises a silicon substrate comprising a first surface; a channel portion over the first surface, wherein the channel portion has a second surface at a first height above the first surface, and a length parallel to first surface; and two source/drain (S/D) regions on the first surface and surrounding the channel portion along the length of the channel portion, wherein the two S/D regions comprise SiGe, Ge, Si, SiC, GeSn, SiGeSn, SiSn, or III-V material.

20 Claims, 12 Drawing Sheets



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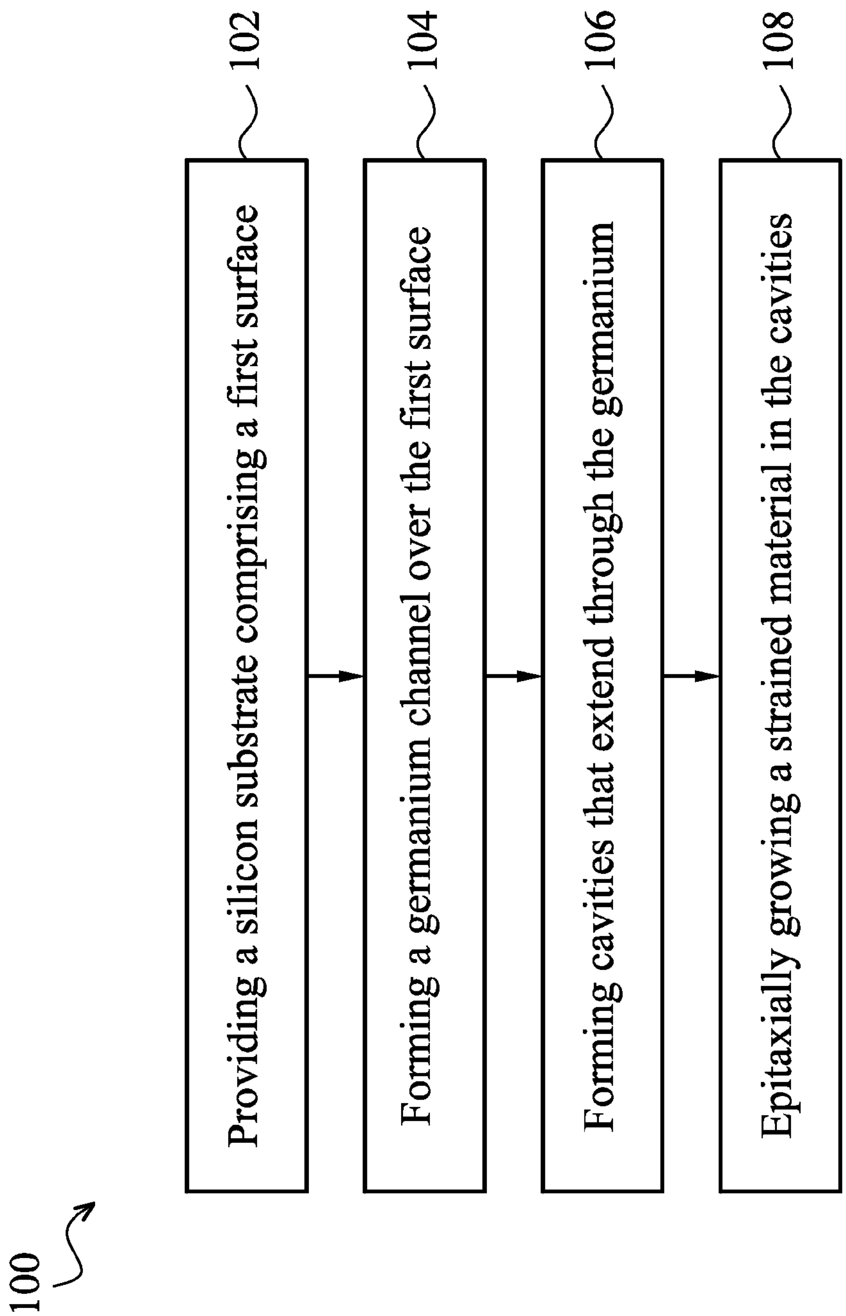

100
102
Providing a silicon substrate comprising a first surface
104
Forming a germanium channel over the first surface
106
Forming cavities that extend through the germanium
108
Epitaxially growing a strained material in the cavities

FIG. 1

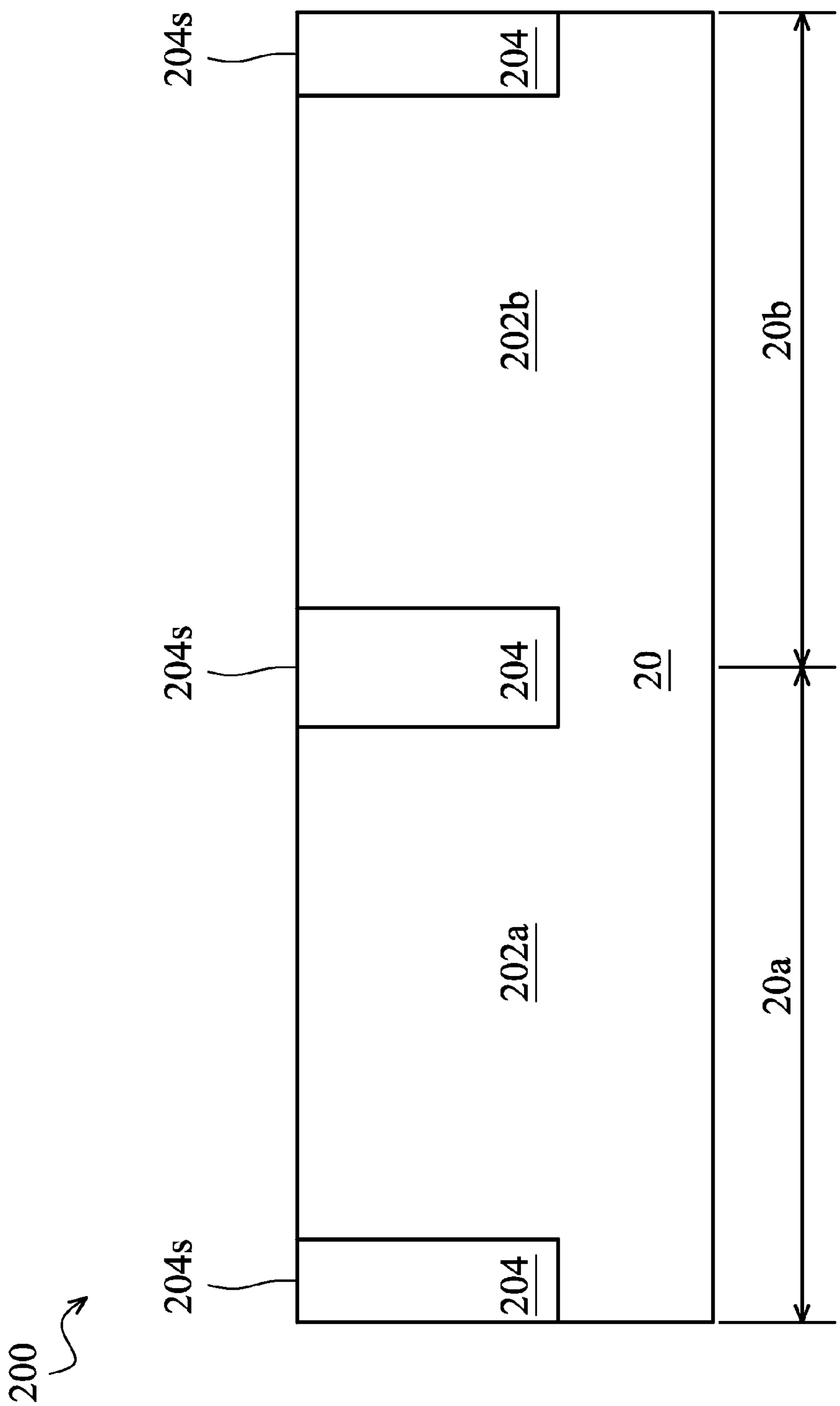


FIG. 2A

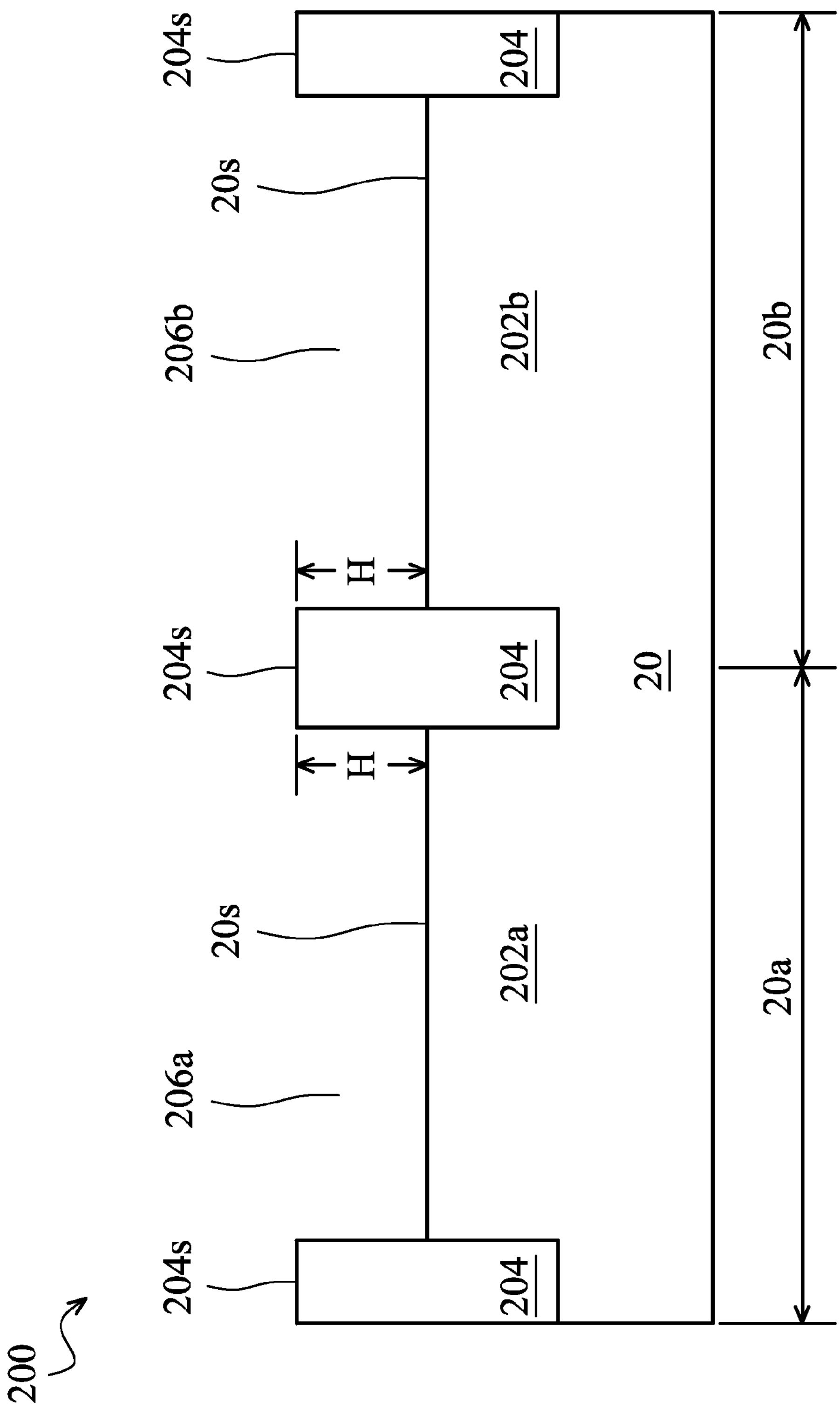

204s
20s
206b
204s
20s
206a
204s
200
204
202b
H
204
20
H
202a
204
20b
20a

FIG. 2B

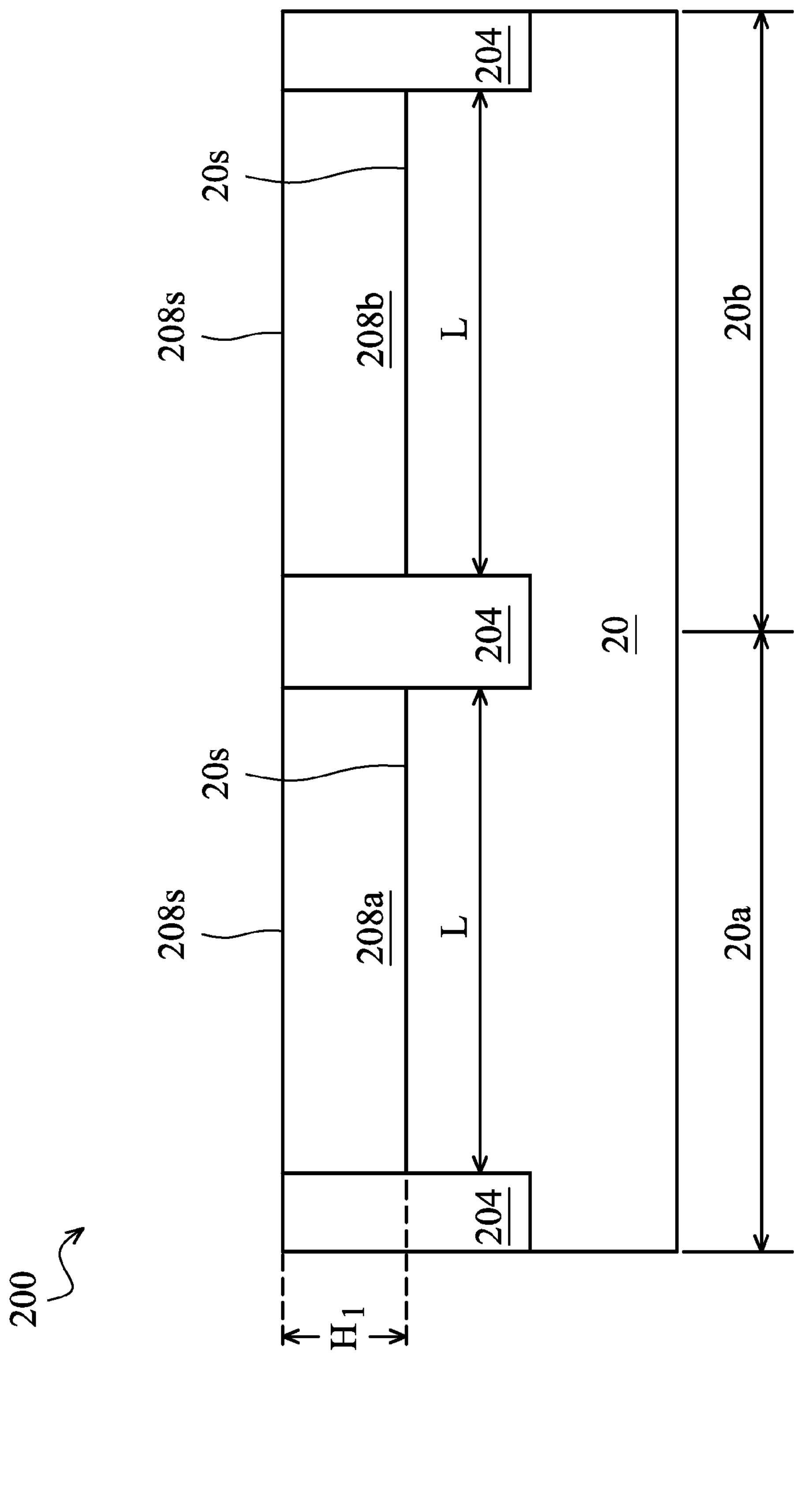
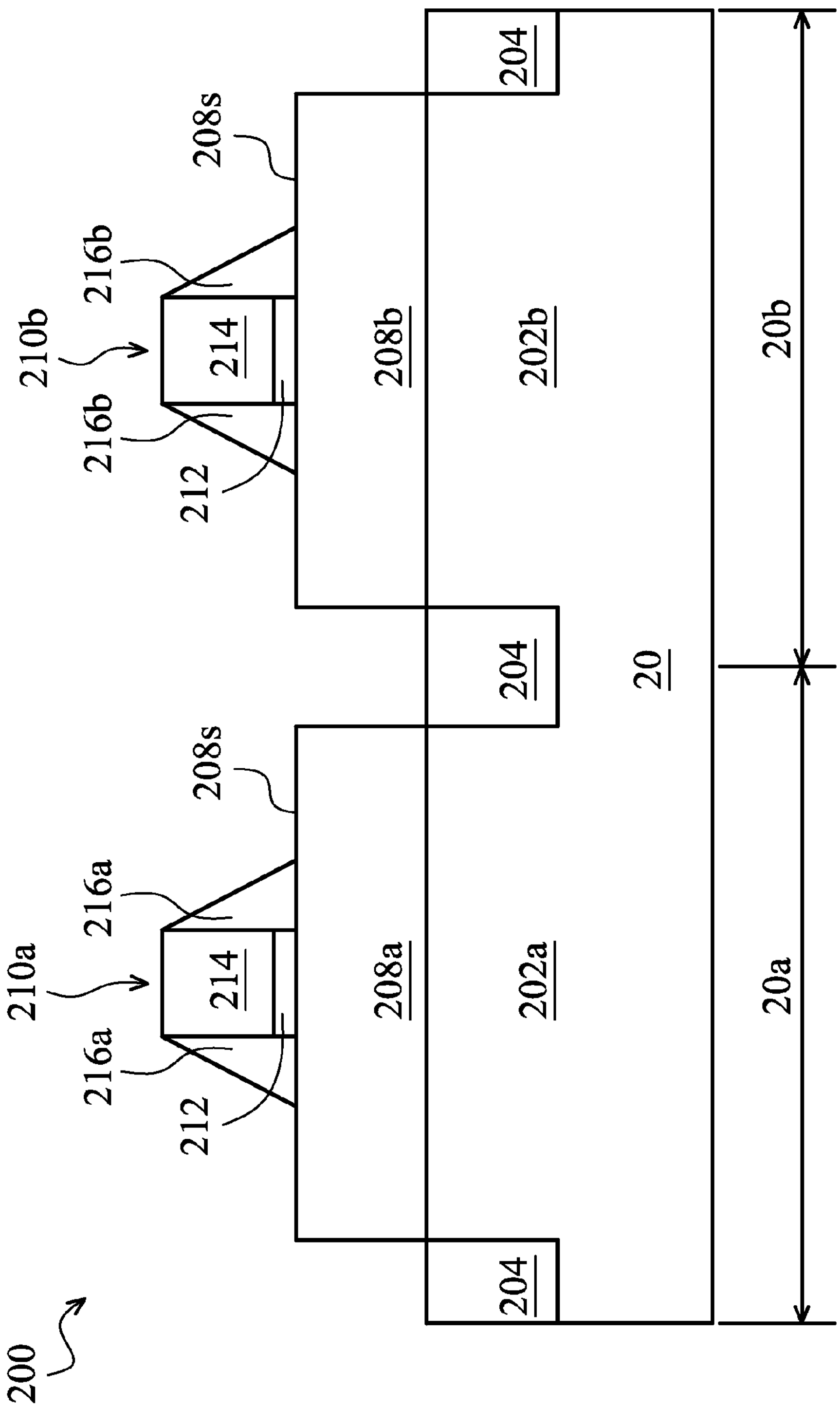


FIG. 2C



200
204
204
204
208s
208s
216a
216a
210a
214
212
208a
202a
20a
216b
216b
210b
214
212
208b
202b
20b
20

FIG. 2D

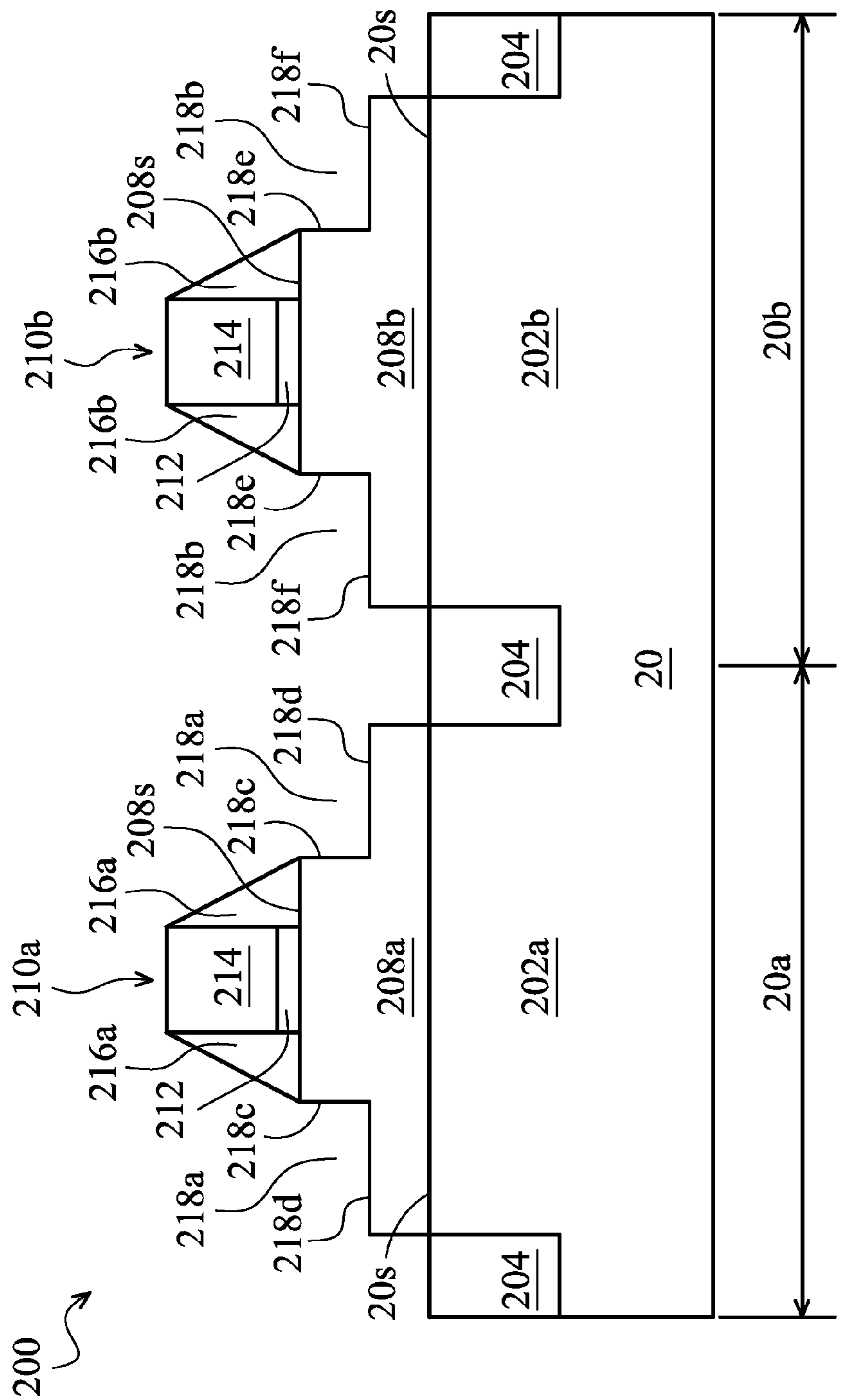

200
210a
210b
214
214
212
212
216a
216a
216b
216b
208s
208s
218a
218a
218b
218b
218c
218c
218d
218d
218e
218e
218f
218f
20s
20s
208a
208b
202a
202b
204
204
204
20
20a
20b

FIG. 2E

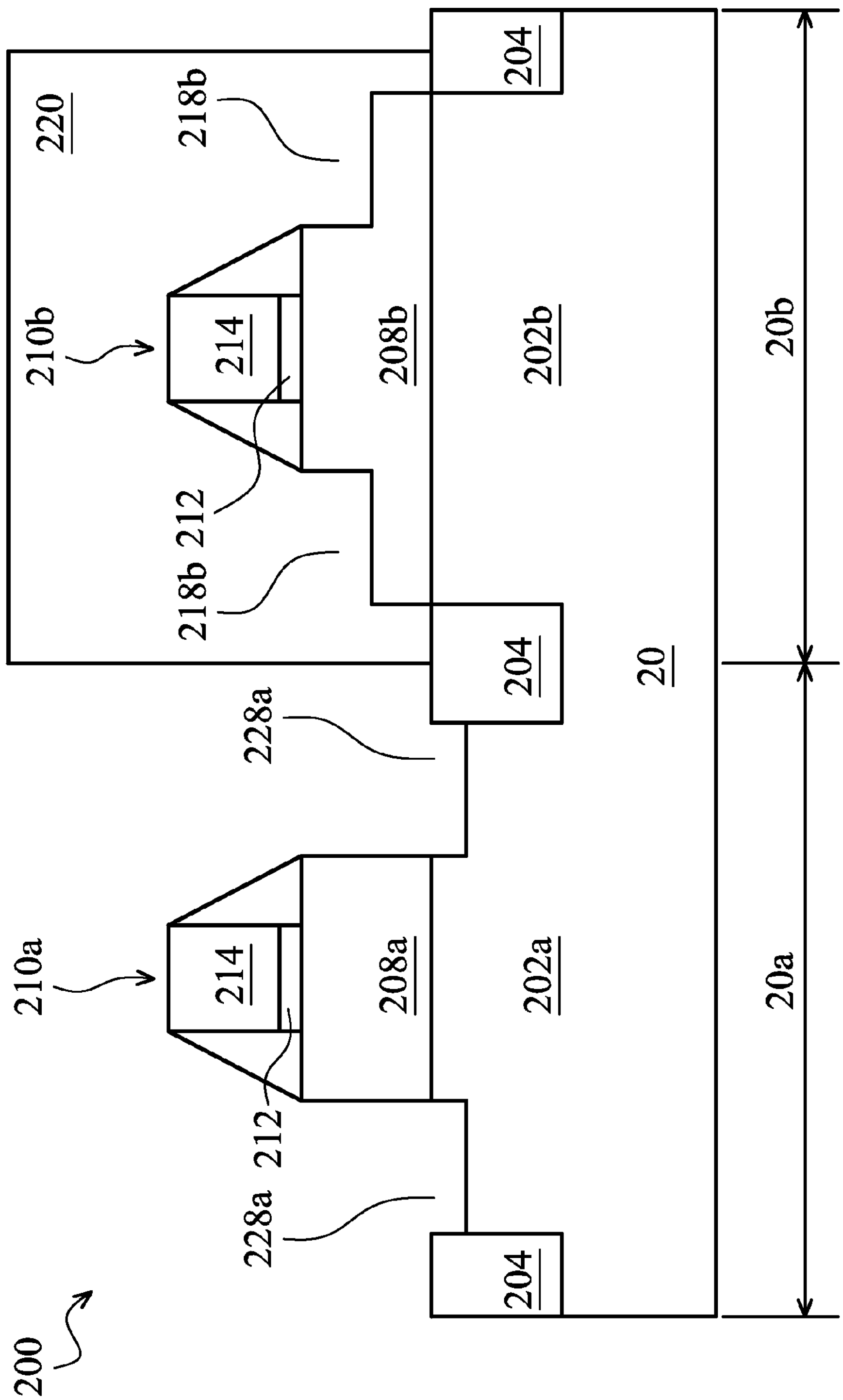

200
204
228a
212
210a
214
208a
202a
20a
228a
204
20
218b
212
210b
214
208b
202b
20b
220
218b
204

FIG. 2F

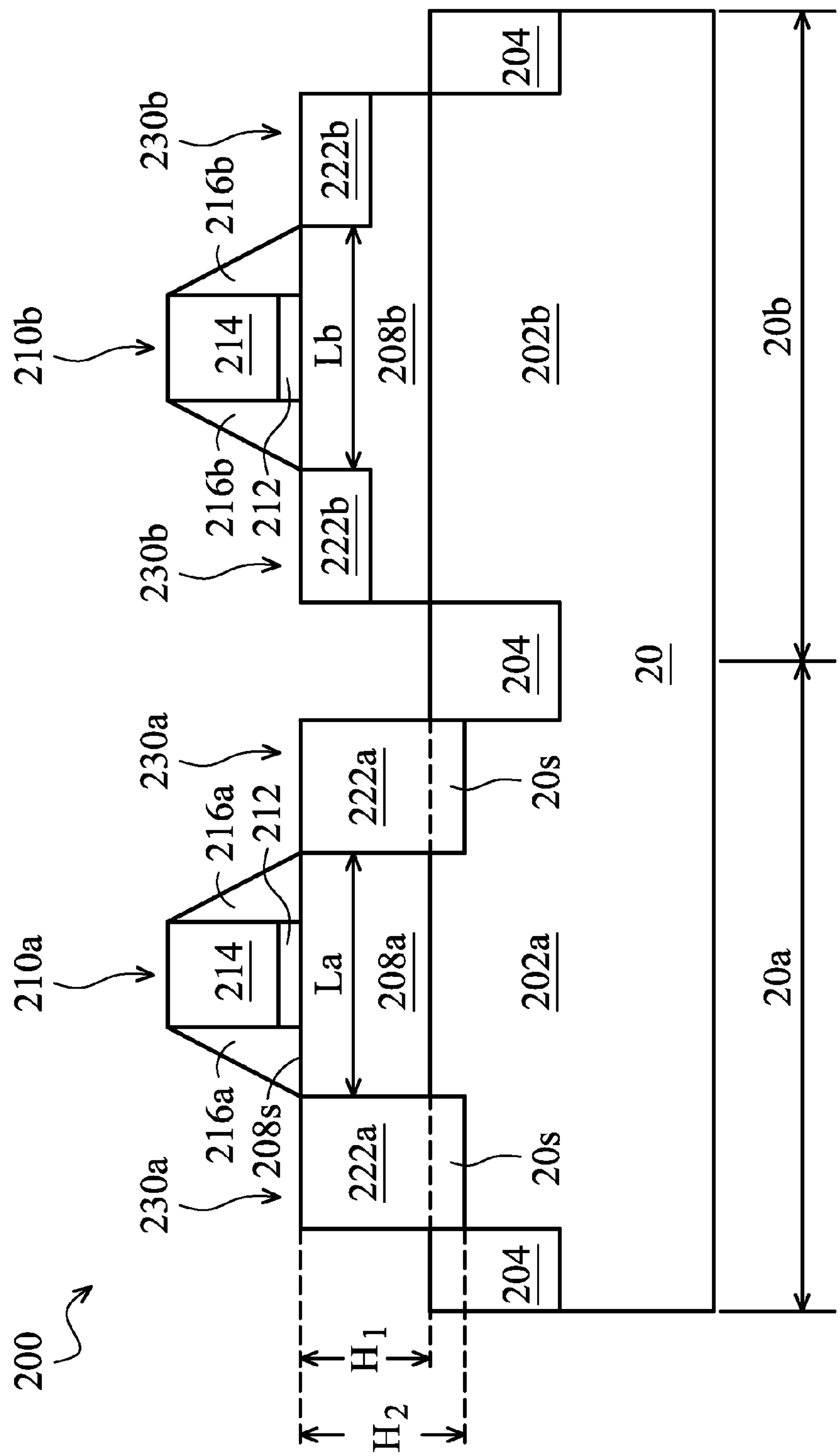

200
230a
230b
210a
210b
216a
216b
208s
212
214
222a
222b
La
Lb
208a
208b
202a
202b
204
20s
20
20a
20b
H_1
H_2

FIG. 2G

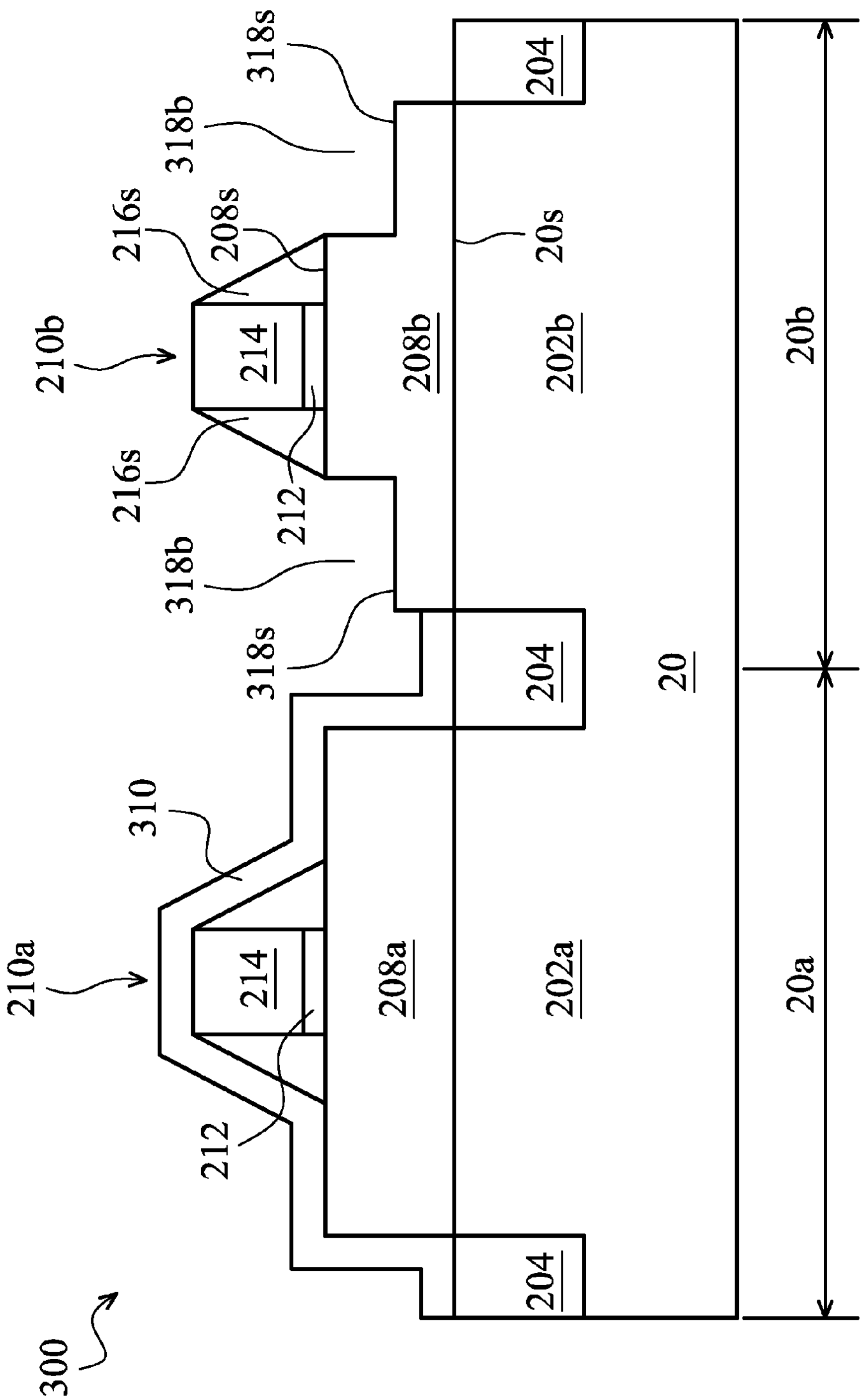

300
210a
310
212
214
208a
202a
204
20a
20
20b
210b
216s
208s
318b
318s
20s
208b
202b

FIG. 3A

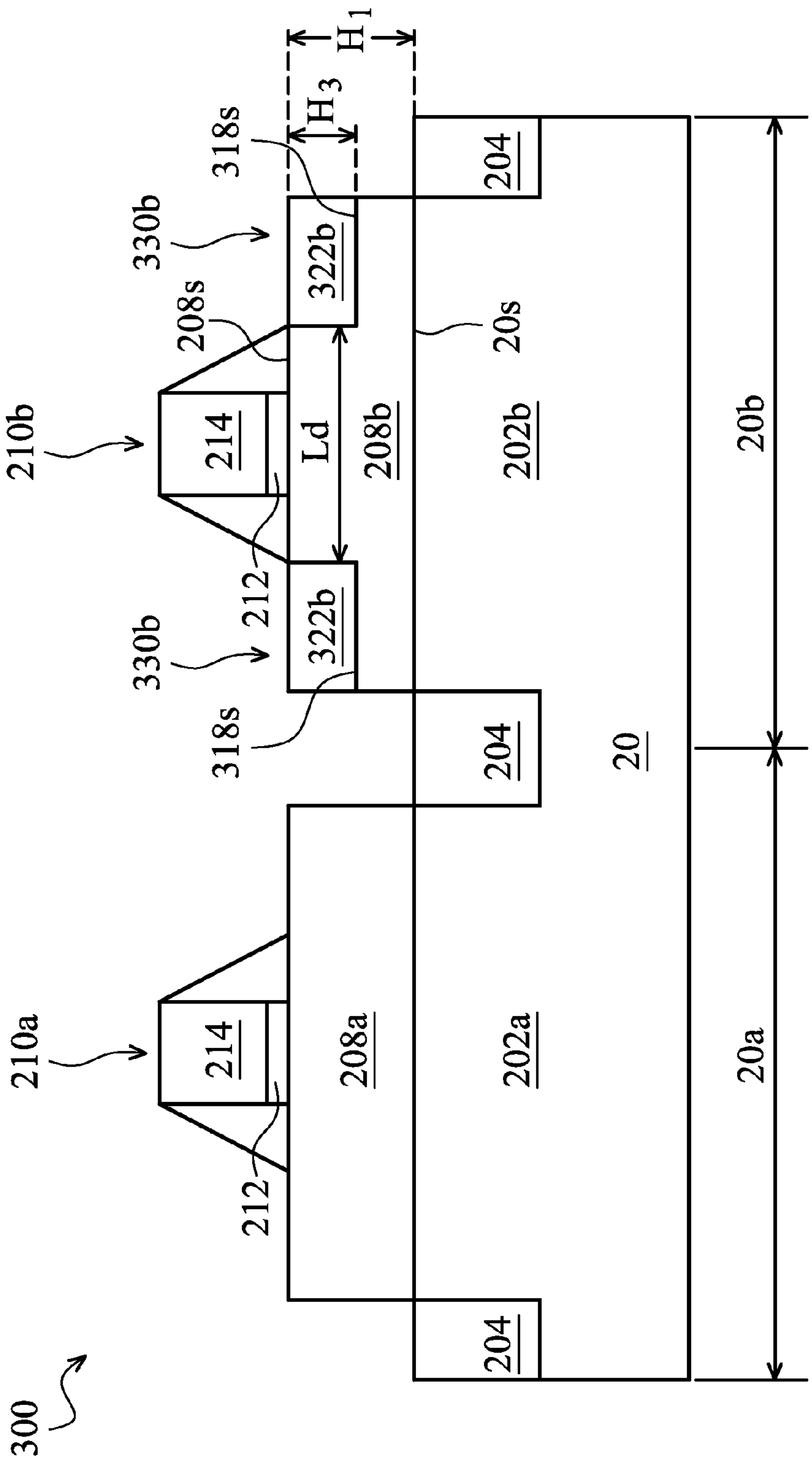

H1
H3
318s
330b
322b
208s
20s
204
210b
214
Ld
208b
202b
20b
212
330b
322b
318s
204
20
210a
214
208a
202a
20a
212
204
300

FIG. 3B

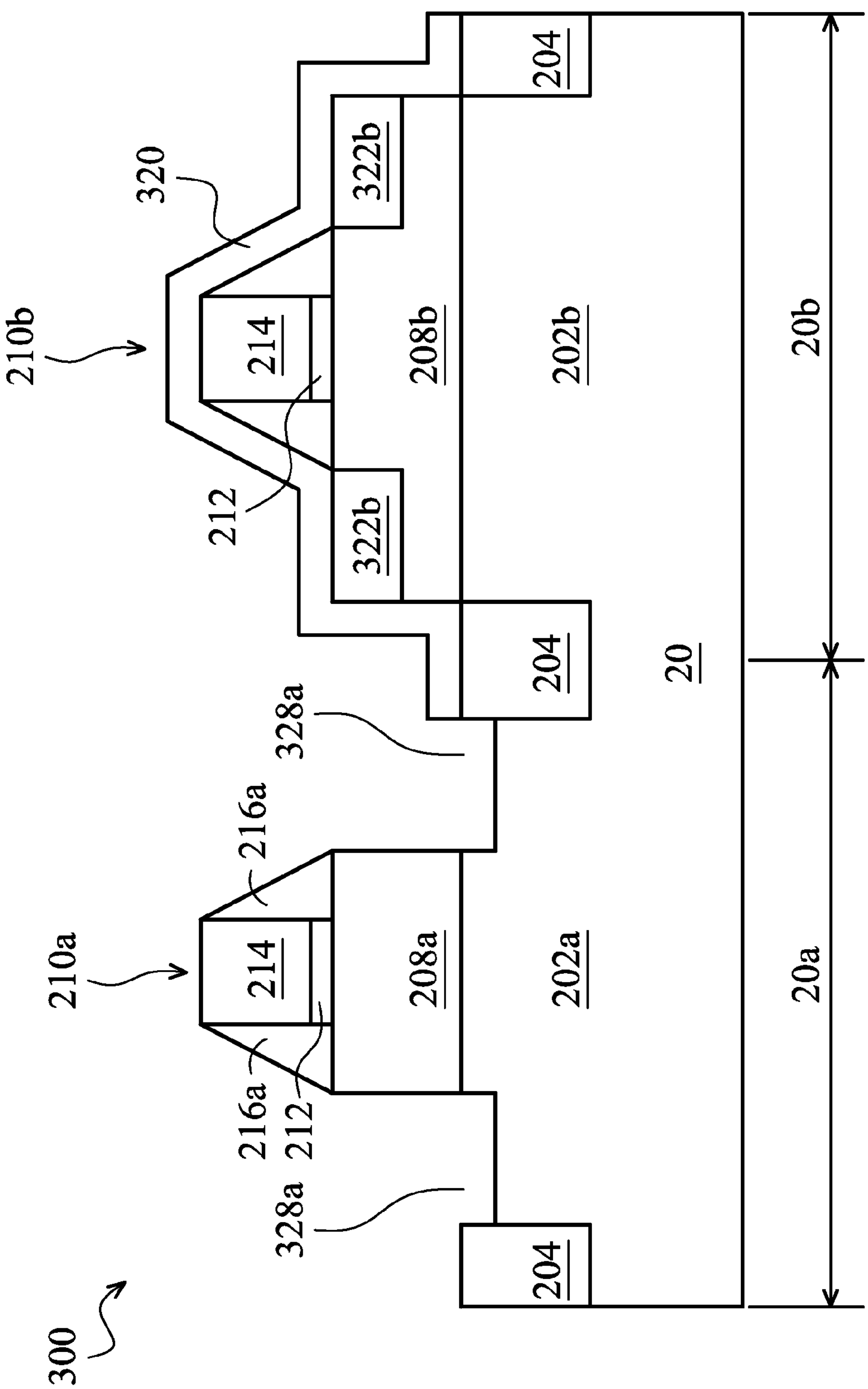

300
210a
210b
320
214
214
212
212
216a
216a
208a
208b
202a
202b
204
204
204
322b
322b
328a
328a
20
20a
20b

FIG. 3C

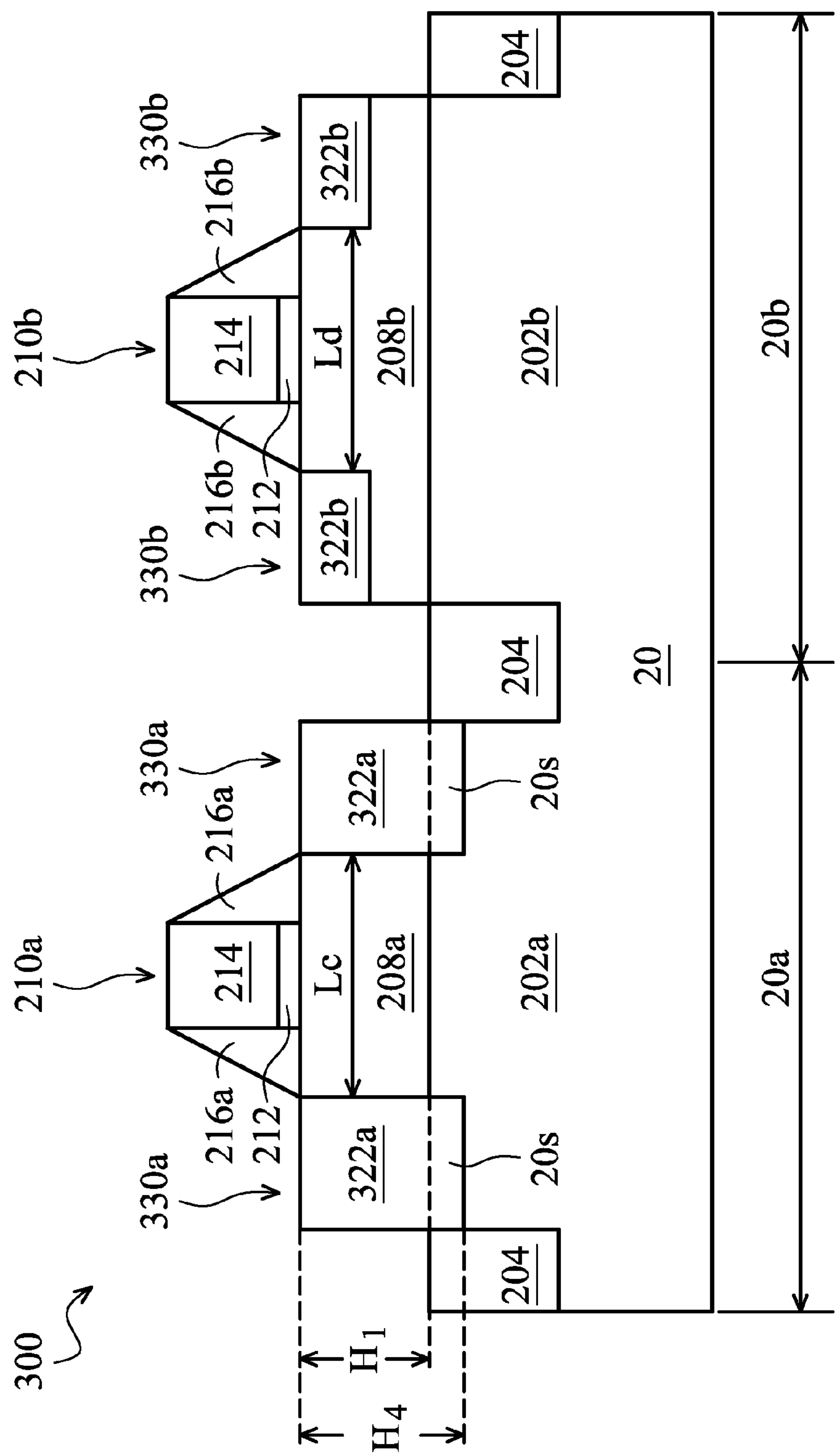

300
330a
216a
212
322a
20s
204
H1
H4
210a
214
Lc
208a
202a
20a
20
330b
216b
322b
210b
Ld
208b
202b
20b

FIG. 3D

STRAINED STRUCTURE OF SEMICONDUCTOR DEVICE AND METHOD OF MAKING THE STRAINED STRUCTURE

CROSS-REFERENCE TO RELATED APPLICATION

The present application claims priority of U.S. Provisional Patent Application Ser. No. 61/638,175, filed on Apr. 25, 2012, which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

This disclosure relates to integrated circuit fabrication and, more particularly, to a semiconductor device with a strained structure.

BACKGROUND

When a semiconductor device, such as a metal-oxide-semiconductor field-effect transistor (MOSFET), is scaled down through various technology nodes, high-k gate dielectric layer and metal gate electrode layer are incorporated into the gate stack of the MOSFET to improve device performance with the decreased feature sizes. In addition, strained structures in source and drain (S/D) recess cavities of the MOSFET utilizing selectively grown silicon germanium (SiGe) may be used to enhance carrier mobility.

However, there are challenges to implement such features and processes in complementary metal-oxide-semiconductor (CMOS) fabrication. For example, it is difficult to achieve enhanced carrier mobility for a field-effect transistor (FET) because strained materials can not deliver a given amount of strain into channel region of the FET, thereby increasing the likelihood of device instability and/or device failure. As the gate length and spacing between devices decrease, these problems are exacerbated.

BRIEF DESCRIPTION OF THE DRAWINGS

The present disclosure is best understood from the following detailed description when read with the accompanying figures. It is emphasized that, in accordance with the standard practice in the industry, various features are not drawn to scale and are used for illustration purposes only. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

FIG. **1** is a flowchart of a method of fabricating a strained structure of a semiconductor device according to various aspects of the present disclosure;

FIGS. **2**A-**2**G are schematic cross-sectional views of an example semiconductor device comprising a strained structure at various stages of fabrication according to various aspects of the present disclosure; and

FIGS. **3**A-**3**D are schematic cross-sectional views of another example semiconductor device comprising a strained structure at various stages of fabrication according to various aspects of the present disclosure.

DESCRIPTION

It is understood that the following disclosure provides many different embodiments, or examples, for implementing different features of the invention. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

Referring to FIG. **1**, illustrated is a flowchart of a method **100** of fabricating a strained structure of a semiconductor device according to various aspects of the present disclosure. The method **100** begins with step **102** in which a silicon substrate comprising a first surface is provided. The method **100** continues with step **104** in which a germanium channel is formed over the first surface. The method **100** continues with step **106** in which a cavity is formed that extends through the germanium channel and into the silicon substrate. The method **100** continues with step **108** in which a strained material is epitaxially-grown in the cavity. The discussion that follows illustrates embodiments of semiconductor devices that can be fabricated according to the method **100** of FIG. **1**.

FIGS. **2**A-**2**G are schematic cross-sectional views of an example semiconductor device **200** comprising a strained structure **230***a* at various stages of fabrication according to various aspects of the present disclosure. FIGS. **3**A-**3**D are schematic cross-sectional views of another example semiconductor device **300** comprising a strained structure **330***a* at various stages of fabrication according to various aspects of the present disclosure. As employed in the present disclosure, the term semiconductor devices **200**, **300** refer to a fin field effect transistor (FinFET). The FinFET refers to any fin-based, multi-gate transistor. In some alternative embodiments, the term semiconductor devices **200**, **300** refer to a planar field effect transistor (FET). The semiconductor devices **200**, **300** may be included in a microprocessor, memory cell, and/or other integrated circuit (IC). It is noted that the method of FIG. **1** does not produce a completed semiconductor devices **200**, **300**. Completed semiconductor devices **200**, **300** may be fabricated using complementary metal-oxide-semiconductor (CMOS) technology processing. Accordingly, it is understood that additional processes may be provided before, during, and after the method **100** of FIG. **1**, and that some other processes may only be briefly described herein. Also, FIGS. **2**A through **3**D are simplified for a better understanding of the concepts of the present disclosure. For example, although only the semiconductor devices **200**, **300** are depicted in FIGS. **2**A-**3**D, it is understood the IC may comprise a number of other devices comprising resistors, capacitors, inductors, fuses, etc.

Referring to FIG. **2**A and step **102** in FIG. **1**, a substrate **20** is provided. In one embodiment, the substrate **20** comprises a crystalline silicon substrate (e.g., wafer). In an alternative embodiment, the substrate **20** may be made of some other suitable elemental semiconductor, such as diamond or germanium; a suitable compound semiconductor, such as gallium arsenide, silicon carbide, indium arsenide, or indium phosphide; or a suitable alloy semiconductor, such as silicon germanium carbide, gallium arsenic phosphide, or gallium indium phosphide. Further, the substrate **20** may include an epitaxial layer (epi-layer), may be strained for performance enhancement, and/or may include a silicon-on-insulator (SOI) structure. The substrate **20** may comprise various doped regions depending on design requirements (e.g., p-type substrate or n-type substrate). In some embodiments, the doped regions may be doped with p-type or n-type dopants. For example, the doped regions may be doped with p-type dopants, such as boron or BF_2; n-type dopants, such as phosphorus or arsenic; and/or combinations thereof. The doped regions may be usable for forming an n-type field effect transistor (FET), or alternatively for forming a p-type FET.

In the depicted embodiment, the substrate **20** comprises a first region **20***a* and a second region **20***b*. In one embodiment for the semiconductor device **200**, the first region **20***a* refers to a core region where core devices would be formed. The second region **20***b* refers to a peripheral region where input/output (I/O) devices would be formed. In some embodiments, both the core devices and I/O devices are p-type FETs. In some embodiments, both the core devices and I/O devices are n-type FETs. In an alternative embodiment for the semiconductor device **300**, the first region **20***a* refers to a first core region where first core devices would be formed. The second region **20***b* refers to a second core region where second core devices would be formed. In the depicted embodiment, the first core devices are p-type FETs, while the second core devices are n-type FETs. In yet another alternative embodiment for the semiconductor device **300**, the first region **20***a* refers to a first core region where first core devices would be formed. The second region **20***b* refers to a peripheral region where I/O devices would be formed. In the depicted embodiment, the first core devices are p-type FETs, while the I/O devices are n-type FETs.

In an embodiment for forming FinFETs, the substrate **20** comprises a first fin structure **202***a* in the first region **20***a* and a second fin structure **202***b* in the second region **20***b*. Each of the first fin structure **202***a* and second fin structure **202***b*, formed on the substrate **20**, comprises one or more fins. In the depicted embodiment, for simplicity, each of the first fin structure **202***a* and second fin structure **202***b* comprises a single fin.

The first and second fin structures **202***a*, **202***b* are formed using any suitable process comprising various deposition, photolithography and/or etching processes. An exemplary photolithography process may include forming a photoresist layer (resist) overlying the substrate **20** (e.g., on a silicon layer), exposing the resist to a pattern, performing a post-exposure bake process, and developing the resist to form a masking element including the resist. The silicon layer may then be etched using reactive ion etching (RIE) processes and/or other suitable processes. In an example, silicon fins of the first and second fin structures **202***a*, **202***b* may be formed using patterning and etching a portion of the silicon substrate **20**. In another example, silicon fins of the first and second fin structures **202***a*, **202***b* may be formed using patterning and etching a silicon layer deposited overlying an insulator layer (for example, an upper silicon layer of a silicon-insulator-silicon stack of an SOI substrate).

In the depicted embodiment, isolation regions are formed within the substrate **20** to define and electrically isolate the first and second fin structures **202***a*, **202***b*. In one example, the isolation regions include a shallow trench isolation (STI) **204** regions. The isolation regions may comprise silicon oxide, silicon nitride, silicon oxynitride, fluoride-doped silicate glass (FSG), a low-K dielectric material, and/or combinations thereof. The isolation regions, and in the present embodiment, the STI **204** regions, may be formed by any suitable process. As one example, the formation of the STI **204** regions may include filling trenches between the first and second fin structures **202***a*, **202***b* (for example, using a chemical vapor deposition process) with a dielectric material. In some embodiments, the filled trench may have a multi-layer structure such as a thermal oxide liner layer filled with silicon nitride or silicon oxide. In the depicted embodiment, the STI **204** regions comprise STI surfaces **204***s*.

Referring to FIG. **2**B and step **102** in FIG. **1**, upper portion of the first fin structure **202***a* is recessed to form first trench **206***a* below the STI surfaces **204***s*, while upper portion of the second fin structure **202***b* is recessed to form second trench **206***b* below the STI surfaces **204***s*. In the present embodiment, each of exposed surfaces of lower portions of the first and second fin structures **202***a*, **202***b* defines a first surface **20***s*. In an exemplary embodiment, a height H of the first and second trenches **206***a*, **206***b* may range from about 20 nm to about 70 nm. One skilled in the art will realize, however, that the dimensions and values recited throughout the descriptions are merely examples, and may be changed to suit different scales of ICs.

In the depicted embodiment, using the STI **204** regions as a hard mask, a biased etching process is performed to recess the first fin structure **202***a* to form the first trench **206***a* and the second fin structure **202***b* to form the second trench **206***b*. In one embodiment, the etching process may be performed under a pressure of about 1 mTorr to 1000 mTorr, a power of about 50 W to 1000 W, a bias voltage of about 20 V to 500 V, at a temperature of about 40° C. to 60° C., using a HBr and/or Cl_2 as etch gases. Also, in some embodiments, the bias voltage used in the etching process may be tuned to allow better control of an etching direction to achieve predetermined profiles for the trenches **206***a*, **206***b*.

The method **100** continues with step **104** in which the structure in FIG. **2**C is produced by forming a first germanium channel **208***a* and a second germanium channel **208***b* over the first surface **20***s*, wherein each of the first germanium channel **208***a* and the second germanium channel **208***b* has a second surface **208***s* at a first height H_1 above the first surface **20***s*, and a length L parallel to first surface **20***s*.

When choosing a semiconductor material for forming a channel region, considerations include the properties of the semiconductor material such as junction forward voltage, mobility of electron and hole, leakage current level, and quality of interface between the semiconductor material and other materials, such as oxide materials. Germanium (Ge) has higher electron mobility than Si. Accordingly, in the depicted embodiment, a channel region of the semiconductor device **200** is Ge. In some embodiments, the semiconductor material for forming the channel region comprises a material other than germanium, such as gallium arsenide, silicon carbide, indium arsenide, or indium phosphide; or a suitable alloy semiconductor, such as silicon germanium carbide, gallium arsenic phosphide, or gallium indium phosphide.

In one embodiment, the Ge epitaxial process may be performed under a pressure of about 10 mTorr to 100 mTorr, at a temperature of about 350° C. to 450° C., using GeH_4, GeH_3CH_3, and/or $(GeH_3)_2CH_2$ as epitaxial gases. Optionally, an anneal process after the epitaxial process is performed at a temperature of about 550° C. to 750° C. to confine dislocation defects on the interface of the Si and Ge epitaxial layer. In an embodiment for forming planar FETs (not shown), the portion of the STI **204** remains due to only surface channel needed. In an embodiment for forming FinFETs, a portion of the STI **204** regions is removed by HF solution to expose the Ge epitaxial layer (shown in FIG. **2**D), acting as germanium channels of the semiconductor devices **200**, **300**.

Referring to FIG. **2**D, subsequent to the formation of the first and second germanium channels **208***a*, **208***b* over the first surface **20***s*, a first gate stack **210***a* is formed on the second surface **208***s* of the first germanium channels **208***a*, while a second gate stack **210***b* is formed on the second surface **208***s* of the second germanium channels **208***b*. In the depicted embodiment, each of the first and second gate stacks **210***a*, **210***b* comprises a gate dielectric layer **212** and a gate electrode layer **214**. The first and second gate stacks **210***a*, **210***b* may be formed using any suitable process, including the processes described herein.

In one example, the gate dielectric layer **212** and gate electrode layer **214** are sequentially deposited over the substrate **20**. In some embodiments, the gate dielectric layer **212** may include silicon oxide, silicon nitride, silicon oxy-nitride, or high-k dielectric. High-k dielectrics comprise metal oxides. Examples of metal oxides used for high-k dielectrics include oxides of Li, Be, Mg, Ca, Sr, Sc, Y, Zr, Hf, Al, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu, or mixtures thereof. In the present embodiment, the gate dielectric layer **212** is a high-k dielectric layer with a thickness in the range of about 10 to 30 angstroms. The gate dielectric layer **212** may be formed using a suitable process such as atomic layer deposition (ALD), chemical vapor deposition (CVD), physical vapor deposition (PVD), thermal oxidation, UV-ozone oxidation, or combinations thereof. The gate dielectric layer **212** may further comprise an interfacial layer (not shown) to reduce damage between the gate dielectric layer **212** and the fin structures **202***a* and **202***b*. The interfacial layer may comprise silicon oxide.

In some embodiments, the gate electrode layer **214** may comprise a single layer or multilayer structure. In the present embodiment, the gate electrode layer **214** may comprise poly-silicon. Further, the gate electrode layer **214** may be doped poly-silicon with the uniform or non-uniform doping. In some alternative embodiments, the gate electrode layer **214** may include a metal such as Al, Cu, W, Ti, Ta, TiN, TiAl, TiAlN, TaN, NiSi, CoSi, other conductive materials with a work function compatible with the substrate material, or combinations thereof. In the present embodiment, the gate electrode layer **214** has a thickness in the range of about 30 nm to about 60 nm. The gate electrode layer **214** may be formed using a suitable process such as ALD, CVD, PVD, plating, or combinations thereof.

Then, a layer of photoresist (not shown) is formed over the gate electrode layer **214** by a suitable process, such as spin-on coating, and patterned to form a patterned photoresist feature by a proper lithography patterning method. In at least one embodiment, a width of the patterned photoresist feature is in the range of about 5 to 45 nm. The patterned photoresist feature can then be transferred using a dry etching process to the underlying layers (i.e., the gate electrode layer **214** and the gate dielectric layer **212**) to form the first and second gate stacks **210***a*, **210***b*. The photoresist layer may be stripped thereafter.

In another example, a hard mask layer (not shown) is formed over the gate electrode layer **214**; a patterned photoresist layer (not shown) is formed on the hard mask layer; the pattern of the photoresist layer is transferred to the hard mask layer and then transferred to the gate electrode layer **214** and the gate dielectric layer **212** to form the first and second gate stacks **210***a*, **210***b*. The hard mask layer comprises silicon oxide. In some alternative embodiments, the hard mask layer may optionally comprise silicon nitride, silicon oxynitride, and/or other suitable dielectric materials, and may be formed using a method such as CVD or PVD. The hard mask layer has a thickness in the range from about 100 to 800 angstroms. The photoresist layer may be stripped thereafter.

Still referring to FIG. **2**D, the semiconductor device **200** further comprises a pair of sidewall spacers **216***a* on two sides of the first gate stack **210***a* and a pair of sidewall spacers **216***b* on two sides of the second gate stack **210***b*. In some embodiments, the sidewall spacers **216***a* are formed by first forming a dielectric layer over the first and second gate stacks **210***a*, **210***b*. The dielectric layer may include silicon oxide, silicon nitride, silicon oxy-nitride, or other suitable material. The dielectric layer may comprise a single layer or multilayer structure. The dielectric layer may be formed by CVD, PVD, ALD, or other suitable technique. The dielectric layer has a thickness ranging from about 5 to 15 nm. Then, an anisotropic etching is performed on the dielectric layer to form the pair of sidewall spacers **216***a* on two sides of the first gate stack **210***a* and the pair of sidewall spacers **216***b* on two sides of the second gate stack **210***b*.

Referring to FIG. **2**E, after the formation of the first and second gate stacks **210***a*, **210***b*, portions of the first and second germanium channels **208***a*, **208***b* (other than where the first and second gate stacks **210***a*, **210***b* and sidewall spacers **216***a*, **216***b* are formed thereover) are recessed to form first source and drain (S/D) cavities **218***a* in the first germanium channels **208***a* and second S/D cavities **218***b* in the second germanium channels **208***b*. Both the first and second S/D cavities **218***a*, **218***b* are between the first surface **20***s* and second surface **208***s*. In the depicted embodiment, the first S/D cavities **218***a* are adjacent to the first gate stack **210***a*, while the second S/D cavities **218***b* are adjacent to the second gate stack **210***b*, wherein each first S/D cavities **218***a* formed by the first germanium channel **208***a* comprises one sidewall **218***c* and a bottom surface **218***d*, wherein each second S/D cavities **218***b* formed by the second germanium channel **208***b* comprises one sidewall **218***e* and a bottom surface **218***f*. In an alternative embodiment, the germanium channels **208***a*, **208***b* are not all recessed as depicted in FIG. **2**E.

In the depicted embodiment, using the pairs of sidewall spacers **216***a*, **216***b* as hard masks, a biased etching process is performed to recess at least a portion of the second surface **208***s* of the first and second germanium channels **208***a*, **208***b* that are unprotected or exposed to form the first and second S/D cavities **218***a*, **218***b*. In one embodiment, the etching process may be performed using a chemical selected from NF_3, CF_4, and SF_6 as an etching gas. In an alternative embodiment, the etching process may be performed using a solution comprising NH_4OH and H_2O_2.

The process steps up to this point have provided the first and second S/D cavities **218***a*, **218***b* between the first surface **20***s* and second surface **208***s*. In some configurations, using a metal-organic chemical vapor deposition (MOCVD) process, a strained material such as a gallium arsenide (GaAs) is selectively grown in the first cavities **218***a* of the first germanium channels **208***a* along the sidewall **208***c* and the bottom surface **208***d*. However, the growing process of the strained material is not well-controlled using the MOCVD process.

Therefore, using MOCVD creates a non-uniform distribution of strained material in the cavities **218***a*. Since the lattice constant of the strained material is different from the first germanium channels **208***a*, the channel region of a semiconductor device is strained or stressed to enhance carrier mobility of the device. However, the non-uniform distribution of strained materials in the cavities **218***a* causes non-uniformity of strains applied to the channel region of the semiconductor device. Thus, the strained material may not deliver a given amount of strain into channel region of the semiconductor device, resulting in an insufficient on-current of the semiconductor device.

Accordingly, the processing discussed below with reference to FIGS. **2**F-**2**G and **3**A-**3**D may form cavities that extend through the germanium channel and into the silicon substrate. The cavities are filled with a strained structure comprising a SiGe layer. The strained structure may decrease non-uniform distribution of strained material, thereby delivering a given amount of strain into channel region of the semiconductor device. Problems associated with insufficient on-current of a semiconductor device may be avoided, thereby enhancing the device performance.

For fabricating one embodiment of a strained structure **230** (shown in FIG. **2**G) of the semiconductor device **200**, the structure in FIG. **2**F is produced by a deep-cavity patterning process (step **106** in FIG. **1**). The deep-cavity patterning process may be accomplished by forming a photo-sensitive layer **220** over the substrate **20**. The photo-sensitive layer **220** is then patterned to expose the first S/D cavities **218***a* of the first germanium channel **208***a*, while cover the second S/D cavities **218***b* of the second germanium channel **208***b*.

In the depicted embodiment, using the patterned photo-sensitive layer **220**, first gate stack **210***a*, and STI **204** regions as masks, the exposed first S/D cavities **218***a* of the first germanium channel **208***a* are further etched to form third cavities **228***a* that extend through the first germanium channel **208***a* and into the silicon substrate **20**. In one embodiment, the etching process may be performed using a chemical selected from NF_3, CF_4, and SF_6 as an etching gas. In an alternative embodiment, the etching process may be performed using a solution comprising NH_4OH and H_2O_2. The patterned photo-sensitive layer **220** may be stripped thereafter to expose the second S/D cavities **218***b* of the second germanium channel **208***b*.

Referring to FIG. **2**G and step **108** in FIG. **1**, after formation of the third cavities **228***a* that extend through the first germanium channel **208***a* and into the silicon substrate **20**, the structure in FIG. **2**G is produced by epitaxially-growing a strained material in the second S/D cavities **218***b* to form S/D regions **222***b* and third S/D cavities **228***a* to form S/D regions **222***a*. The strained material may comprises SiGe, Ge, Si, SiC, GeSn, SiGeSn, SiSn, or III-V material.

In the depicted embodiment, a pre-cleaning process may be performed to clean the second and third S/D cavities **218***b*, **228***a* with HF or other suitable solution. Then, the strained material such as silicon germanium (SiGe) is selectively grown by an LPCVD process to fill the second and third S/D cavities **218***b*, **228***a*. In the depicted embodiment, the LPCVD process is performed at a temperature of about 660 to 700° C. and under a pressure of about 13 to 50 Torr, using SiH_2Cl_2, HCl, GeH_4, B_2H_6, and H_2 as reaction gases. A ratio of a mass flow rate of the SiH_2Cl_2 to a mass flow rate of the HCl is in the range of about 0.8 to 1.5, while a ratio of a mass flow rate of the SiH_2Cl_2 to a mass flow rate of the GeH_4 is in the range of about 10 to 50.

In the first region **20***a* (or refers to a core region), two S/D regions **222***a* are formed on the first surface **20***s* (dotted line) and sandwiching an upper portion of the first germanium channel **208***a* having a length L_a of the channel **208***a*. In some embodiments, the two S/D regions **222***a* extending downward from the second surface **208***s* is coplanar with the first surface **20***s* (dotted line). In some embodiments, the two S/D regions **222***a* extending downward from the second surface **208***s* is lower than the first surface **20***s*. As such, a portion of the two S/D regions **222***a* extending downward from the second surface **208***s* has a second height H_2 equal to or greater than the first height H_1. In some embodiments, a ratio of the second height H_2 to the first height H_1 is from 1 to 1.2. The two S/D regions **222***a* are combined and referred to a strained structure **230***a*. Compared with the strained structure formed by using MOCVD, the strained structure **230***a* has better uniformity, thereby delivering a given amount of strain into channel region of the semiconductor device **200** and enhancing the device performance.

In the second region **20***b* (or refers to a peripheral region), two S/D regions **222***b* are formed on the second germanium channel **208***b* and sandwiching an upper portion of the second germanium channel **208***b* having a length L_b of the channel **208***b*. The two S/D regions **222***b* are combined and referred to a strained structure **230***b*. In some embodiments, the core devices (or the I/O devices) include both NMOS and PMOS. In some embodiments, both the core devices and I/O devices are p-type FETs if the strained material comprises SiGe, Ge, GeSn, SiGeSn, SiSn, or III-V material. In some embodiments, both the core devices and I/O devices are n-type FETs if the strained material comprises SiGe, Si or SiC.

In some alternative embodiments, for fabricating another embodiment of a strained structure **330** (shown in FIG. **3**D) of the semiconductor device **300**, the structure in FIG. **3**A shows the semiconductor device **300** (**200** in FIG. **2**D) after recessing the second germanium channel **208***b* to form fourth S/D cavities **318***b* in the second germanium channels **208***b*. In the present embodiment, the semiconductor device **300** of FIGS. **3**A-**3**D follows the formation of the semiconductor device **200** of FIG. **2**D. Accordingly, similar features in FIGS. **2**D and **3**A-**3**D are numbered the same for the sake of clarity and simplicity. In the depicted embodiment, the fourth S/D cavities **318***b* are adjacent to the second gate stack **210***b*, wherein each fourth S/D cavities **318***b* formed by the second germanium channel **208***b* has a fourth surface **318***s*. The fourth surface **318***s* is between the first surface **20***s* and second surface **208***s*.

In the depicted embodiment, a dummy dielectric layer comprising a material such as silicon oxide is formed over the substrate **20** by a CVD process, and patterned to form a dummy dielectric feature **310** by proper lithography and etch methods. The patterned dummy dielectric feature **310** covers the first germanium channel **208***a* and exposes portions of the second germanium channel **208***b* (other than where the second gate stack **210***b* and the pair of sidewall spacers **216***b* are formed thereover). Then, using the patterned dummy dielectric feature **310** and the pair of sidewall spacers **216***b* as hard masks, a biased etching process is performed to recess the second surface **208***s* of the second germanium channel **208***b* that are unprotected or exposed to form the fourth S/D cavities **318***b* between the first surface **20***s* and the second surface **208***s*. In one embodiment, the etching process may be performed using a chemical selected from NF_3, CF_4, and SF_6 as an etching gas. In an alternative embodiment, the etching process may be performed using a solution comprising NH_4OH and H_2O_2. In some embodiments, the step of recessing the second germanium channel **208***b* as depicted in FIG. **2**E is skipped. In an alternative embodiment, the step of recessing the germanium channels **208***a*, **208***b* in FIG. **2**E is skipped.

Referring to FIG. **3**B, subsequent to formation of the fourth S/D cavities **318***b* between the first surface **20***s* and the second surface **208***s*, two S/D regions **322***b* are epitaxially grown on the fourth surface **318***s* and sandwiching an upper portion of the second germanium channel **208***b* having a length L_d of the second germanium channel **208***b*. In one embodiment, a portion of the two S/D regions **322***b* extending downward from the second surface **208***s* has a third height H_3 less than the first height H_1. In another embodiment, a ratio of the third height H_3 to the first height H_1 is from 0.5 to 0.9. In the depicted embodiment, the two S/D regions **322***b* are combined and referred to a strained structure **330***b*. In some embodiments, the two S/D regions **322***b* comprise SiGe, Si or SiC. As such, the two S/D regions **322***b* in the second region **20***b* refer to a core region for n-type core FETs or a peripheral region for n-type I/O FETs.

In the depicted embodiment, a pre-cleaning process may be performed to clean the fourth S/D cavities **318***b* with HF or other suitable solution. Then, a strained material such as SiC is selectively grown by an LPCVD process to fill the fourth S/D cavities **318***b*. In the depicted embodiment, the LPCVD process is performed at a temperature of about 400 to 800° C. and under a pressure of about 1 to 15 Torr, using SiH_4, CH_4, and H_2 as reaction gases. Then the patterned dummy dielectric feature **310** is removed using HF solution.

Referring to FIG. **3**C and step **106** in FIG. **1**, after the formation of the two S/D regions **322***b* on the fourth surface **318***s*, the structure in FIG. **3**C is produced by recessing the first germanium channel **208***a* to form fifth S/D cavities **328***a* that extend through the first germanium channel **208***a* and into the silicon substrate **20**. In the depicted embodiment, the fifth S/D cavities **328***a* are distributed adjacent to the first gate stack **210***a*.

In the depicted embodiment, a dummy dielectric layer such as silicon oxide is formed over the substrate **20** by a CVD process, and patterned to form a dummy dielectric feature **320** by proper lithography and etch methods. The patterned dummy dielectric feature **320** covers the second germanium channel **208***b* and exposes portions of the first germanium channel **208***a* (other than where the first gate stack **210***a* and the pair of sidewall spacers **216***a* are formed thereover). Then, using the patterned dummy dielectric feature **320** and the pair of sidewall spacers **216***a* as hard masks, a biased etching process is performed to recess the second surface **208***s* of the first germanium channel **208***a* that are unprotected or exposed to form the fifth S/D cavities **328***a*. In at least one embodiment, the etching process may be performed using a chemical selected from NF_3, CF_4, and SF_6 as an etching gas. In an alternative embodiment, the etching process may be performed using a solution comprising NH_4OH and/or H_2O_2.

Referring to FIG. **3**D and step **108** in FIG. **1**, after the formation of the fifth S/D cavities **328***a* that extend through the first germanium channel **208***a* and into the silicon substrate **20**, the structure in FIG. **3**D is produced by epitaxially-growing a strained material in the fifth S/D cavities **328***a* form S/D regions **322***a*. The strained material may comprise SiGe, Ge, GeSn, SiGeSn, SiSn, or III-V material.

In the depicted embodiment, a pre-cleaning process may be performed to clean the fifth S/D cavities **328***a* with HF or other suitable solution. Then, the strained material such as silicon germanium (SiGe) is selectively grown by an LPCVD process to fill the fifth S/D cavities **328***a*. In one embodiment, the LPCVD process is performed at a temperature of about 660 to 700° C. and under a pressure of about 13 to 50 Torr, using SiH_2Cl_2, HCl, GeH_4, B_2H_6, and H_2 as reaction gases. In some embodiments, a ratio of a mass flow rate of the SiH_2Cl_2 to a mass flow rate of the HCl is in the range of about 0.8 to 1.5, while a ratio of a mass flow rate of the SiH_2Cl_2 to a mass flow rate of the GeH_4 is in the range of about 10 to 50.

In the first region **20***a* (or refers to a core region), two S/D regions **322***a* are formed on the first surface **20***s* (dotted line) and sandwiching an upper portion of the first germanium channel **208***a* having a length L_c of the channel **208***a*. In some embodiments, the two S/D regions **322***a* extending downward from the second surface **208***s* is coplanar with the first surface **20***s* (dotted line). In some embodiments, the two S/D regions **322***a* extending downward from the second surface **208***s* is lower than the first surface **20***s*. As such, a portion of the two S/D regions **322***a* extending downward from the second surface **208***s* has a fourth height H_4 equal to or greater than the first height H_1. In some embodiments, a ratio of the fourth height H_4 to the first height H_1 is from 1 to 1.2. The two S/D regions **322***a* are combined and referred to a strained structure **330***a*. Compared with the strained structure formed by using MOCVD, the strained structure **330***a* has better uniformity, thereby delivering a given amount of strain into channel region of the semiconductor device **300** and enhancing the device performance.

After the steps shown in FIG. **1**, as further explained in FIGS. **2**A-**2**G or FIGS. **2**A-**2**D and **3**A-**3**D, have been performed, subsequent processes, comprising silicidation and interconnect processing, are typically performed to complete the semiconductor devices **200**, **300** fabrications.

In accordance with embodiments, a field effect transistor (FET) comprises a silicon substrate comprising a first surface; a channel portion over the first surface, wherein the channel portion has a second surface at a first height above the first surface, and a length parallel to first surface; and two source/drain (S/D) regions on the first surface and surrounding the channel portion along the length of the channel portion, wherein the two S/D regions comprise SiGe, Ge, Si, SiC, GeSn, SiGeSn, SiSn, or III-V material.

In accordance with other embodiments, a semiconductor device comprises a silicon substrate comprising a first surface; a first channel portion and a second channel portion over the first surface, wherein each channel portion has a second surface at a first height above the first surface, and a length parallel to first surface; a first field effect transistor (FET) comprising two SiGe regions on the first surface and surrounding the first channel portion along the length of the first channel portion; and a second FET comprising two SiP regions on a third surface and surrounding the second channel portion along the length of the second channel portion, wherein the third surface is between the first surface and second surface.

In accordance with yet other embodiments, a method of fabricating a field effect transistor (FET) includes providing a silicon substrate comprising a first surface; forming a channel portion over the first surface; and forming cavities that extend through the channel portion and into the silicon substrate; and epitaxially-growing a strained material in the cavities.

While the invention has been described by way of example and in terms of embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.

What is claimed is:

1. A field effect transistor (FET) comprising:

a silicon substrate comprising a first surface;

a channel portion over the first surface, wherein the channel portion has a second surface at a first height above the first surface, a length parallel to the first surface, and the channel portion is a germanium channel portion; and

two source/drain (S/D) regions on the first surface and surrounding the channel portion along the length of the channel portion, wherein the two S/D regions comprise SiGe, Ge, Si, SiC, GeSn, SiGeSn, SiSn, or III-V material,

wherein a portion of each of the two S/D regions extending downward from the second surface is lower than the first surface, thereby defining a second height greater than the first height.

2. The FET of claim **1**, wherein a ratio of the second height to the first height is from 1 to 1.2.

3. The FET of claim **1**, wherein the FET comprises a planar FET.

4. The FET of claim 1, wherein the FET comprises a FinFET.

5. The FET of claim 1, wherein the two S/D regions are combined.

6. A semiconductor device comprising:
a silicon substrate comprising a first surface;
a first channel portion and a second channel portion over the first surface, wherein each channel portion has a second surface at a first height above the first surface, and a length parallel to the first surface;
a first field effect transistor (FET) comprising first two source/drain (S/D) regions on the first surface and surrounding the first channel portion along the length of the first channel portion, wherein the first two S/D regions comprise SiGe, Ge, GeSn, SiGeSn, SiSn, or III-V material; and
a second FET comprising second two S/D regions on a third surface and surrounding the second channel portion along the length of the second channel portion, wherein the third surface is between the first surface and second surface, wherein the second two S/D regions comprise SiGe, Si, or SiC,
wherein a portion of each of the first two S/D regions extending downward from the second surface is lower than the first surface, thereby defining a second height greater than the first height.

7. The semiconductor device of claim 6, wherein a ratio of the second height to the first height is from 1 to 1.2.

8. The semiconductor device of claim 6, wherein a portion of each of the second two S/D regions extending downward from the second surface has a third height less than the first height.

9. The semiconductor device of claim 8, wherein a ratio of the third height to the first height is from 0.5 to 0.9.

10. The semiconductor device of claim 6, wherein the first FET and second FET comprise planar FETs.

11. The semiconductor device of claim 6, wherein the first FET and second FET comprise FinFETs.

12. The semiconductor device of claim 6, wherein the first FET is a p-type FET and the second FET is an n-type FET.

13. The semiconductor device of claim 6, wherein the first FET is a core device and the second FET is an I/O device.

14. The semiconductor device of claim 6, wherein the first two S/D regions are combined.

15. A semiconductor device comprising:
a substrate comprising a first surface;
a first field effect transistor (FET) on the first surface, the first FET comprising:
a first channel portion over the first surface,
first source/drain (S/D) regions on the substrate surrounding the first channel portion along a length of the first channel portion, the first S/D regions having a first height from a second, upper surface to downward extensions lower than the first surface; and
a second FET on the first surface, the second FET comprising:
a second channel portion over the first surface,
second S/D regions on the substrate surrounding the second channel portion along a length of the second channel portion, the second S/D regions having a second height different from the first height.

16. The semiconductor device of claim 15, wherein a portion of the second channel portion is positioned between the first surface and the second S/D regions.

17. The semiconductor device of claim 15, wherein the first channel portion has a channel height above the first surface, wherein a ratio of the first height to the channel height ranges from greater than 1 to 1.2.

18. The semiconductor device of claim 15, wherein the second channel portion has a channel height above the first surface, wherein a ratio of the second height to the channel height ranges from 0.5 to 0.9.

19. The semiconductor device of claim 15, wherein the first channel portion and the second channel portion independently comprise germanium, gallium arsenide, silicon carbide, indium arsenide, indium phosphide, silicon germanium carbide, gallium arsenic phosphide, or gallium indium phosphide.

20. The semiconductor device of claim 15, wherein the first FET comprises a first gate stack on the first channel portion between the first S/D regions, and the second FET comprises a second gate stack on the second channel portion between the second S/D regions.

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